What is Claimed:

1. A process for manufacturing a silicon-on-insulator wafer (10) comprising the steps of:

(a) providing a silicon substrate (4);

(b) forming an oxide insulator layer (2) across the wafer (10), the insulator layer (2) being buried within the silicon substrate (4), dividing the silicon substrate (4) from a top silicon layer (6), and having a top surface (8) and a bottom surface (12);

(c) thickening the insulator layer (2);

(d) creating at least one of a contoured top surface (8a, 8b, 8c, 8d, 8e) and a contoured bottom surface (12e) of the insulator layer (2); and

(e) annealing to further thicken and contour the insulator layer (2).

2. The process of claim 1 wherein the step (b) of forming an oxide insulator layer (2) across the wafer (10) is accomplished using a qualified oxygen implanter (50).

3. The process of claim 2 wherein the step (c) of thickening the insulator layer (2) is accomplished by reducing one or more of the implant dose, energy, and temperature.

4. The process of claim 1 wherein the step (e) of annealing is an oxygen anneal.

5. The process of claim 1 wherein the at least one contoured surface is uniformly convex.

6. The process of claim 5 wherein the step (b) of forming an oxide insulator layer (2) across the wafer (10) is accomplished using a qualified oxygen implanter (50) and the step (d) of creating the at least one uniformly convex surface includes reducing one or more of the implant dose, energy, and temperature to thicken the insulator layer (2) across a preset diameter that is less than the diameter of the wafer (10).

7. The process of claim 1 wherein the at least one contoured surface has alternating convex and substantially flat regions.

8. The process of claim 1 wherein the at least one contoured surface is uniformly concave.

9. The process of claim 8 wherein the step (b) of forming an oxide insulator layer (2) across the wafer (10) is accomplished using a qualified oxygen implanter (50) and the step (d) of creating the at least one uniformly concave surface includes reducing one or more of the implant dose, energy, and temperature to thicken the insulator layer (2) around the wafer (10) in a donut area having an outer diameter not exceeding the diameter of the wafer (10) an interior diameter greater than zero.

10. The process of claim 9 further comprising adjusting the implanter (50) to scan only the donut region around the wafer (10) within preset diameters.

11. The process of claim 1 wherein the at least one contoured surface has alternating concave and substantially flat regions.

12. The process of claim 1 wherein the at least one contoured surface includes a combination of convex, concave, and substantially flat portions.

13. The process of claim 12 wherein the step (b) of forming an oxide insulator layer (2) across the wafer (10) is accomplished using a qualified oxygen implanter (50) and the step (d) of creating the at least one contoured surface includes reducing one or more of the implant dose, energy, and temperature to selectively pattern the buried insulator layer (2) with topography at predetermined coordinates.

14. A process for manufacturing a silicon-on-insulator wafer (10) comprising the steps of:

(a) providing a silicon substrate (4);

(b) forming an oxide insulator layer (2) across the wafer (10), the insulator layer (2) being buried within the silicon substrate (4), dividing the silicon substrate (4) from a top silicon layer (6), and having a top surface (8) and a bottom surface (12);

(c) thickening the insulator layer (2);

(d) generating the chip periodicity for the wafer (10) and setting the coordinates where a predetermined topography of the buried oxide insulator layer (2) is desired;

(e) transferring the coordinates to an oxygen implanter (50) for implementation;

(f) adjusting the energy, dose, or temperature of the oxygen implant with the implanter (50) scanning and the wafer (10) tilting or rotating according to preset coordinates from the chip periodicity map at the predetermined thicknesses and

contours required, thereby creating at least one of a contoured top surface (8a, 8b, 8c, 8d, 8e) and a contoured bottom surface (12e) of the insulator layer (2); and

(g) annealing to further thicken and contour the insulator layer (2).

15. A silicon-on-insulator wafer (10) comprising:

a top silicon layer (6);

a silicon substrate (4); and

an oxide insulator layer (2) disposed across the wafer (10) and between the silicon substrate (4) and the top silicon layer (6), the oxide insulator layer (2) having at least one of a contoured top surface (8a, 8b, 8c, 8d, 8e) and a contoured bottom surface (12e).

16. The silicon-on-insulator wafer (10) of claim 15 wherein the at least one contoured surface (8a) is uniformly convex.

17. The silicon-on-insulator wafer (10) of claim 15 wherein the at least one contoured surface (8b) has alternating convex and substantially flat regions.

18. The silicon-on-insulator wafer (10) of claim 15 wherein the at least one contoured surface (8c) is uniformly concave.

19. The silicon-on-insulator wafer (10) of claim 15 wherein the at least one contoured surface (8d) has alternating concave and substantially flat regions.

20. The silicon-on-insulator wafer (10) of claim 15 wherein the at least one contoured surface (8e, 12e) includes a combination of convex, concave, and substantially flat portions.